![Texas Instruments logo] **TEXAS INSTRUMENTS**

CD4019B Types

CMOS Quad AND/OR Select Gate

High-Voltage Types (20-Volt Rating)

■ CD4019B types consist of four AND/OR select gate configurations, each consisting of two 2-input AND gates driving a single 2-input OR gate. Selection is accomplished by control bits K_a and K_b. In addition to selection of either channel A or channel B information, the control bits can be applied simultaneously to accomplish the logical A + B function.

The CD4019B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).
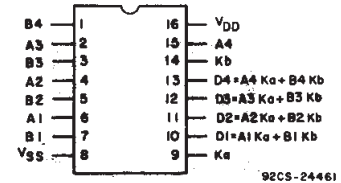
Features:

■ Medium-speed operation . . . . .
· · · t_{PHL} = t_{PLH} = 60 ns (typ.) at C_L = 50 pF, V_{DD} = 10 V
■ Standardized, symmetrical output characteristics
■ 100% tested for quiescent current at 20 V
■ 5-V, 10-V, and 15-V parametric ratings
■ Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"
■ Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
■ Noise margin (full package-temperature range) =
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V

CD4019B FUNCTIONAL DIAGRAM
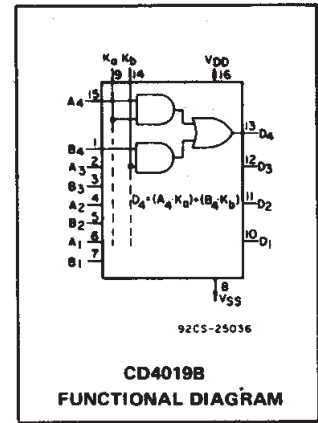
Applications:

■ AND-OR select gating
■ Shift-right/shift-left registers
■ True/complement selection
■ AND/OR/Exclusive-OR selection

MAXIMUM RATINGS, *Absolute–Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
  Voltages referenced to V_{SS} Terminal) . . . . –0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . –0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT . . . . ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
  For T_A = –55°C to +100°C 500mW
  For T_A = +100°C to +125°C. . . . . Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
  FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW
OPERATING-TEMPERATURE RANGE (T_A). . . . . –55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . –65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
  At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max . . . . +265°C

TERMINAL DIAGRAM
Top View

Pin		Pin	
B4	1	16	V_{DD}
A3	2	15	A4
B3	3	14	Kb
A2	4	13	D4 = A4 Ka + B4 Kb
B2	5	12	D3 = A3 Ka + B3 Kb
A1	6	11	D2 = A2 Ka + B2 Kb
B1	7	10	D1 = A1 Ka + B1 Kb
V_{SS}	8	9	Ka

TRUTH TABLE

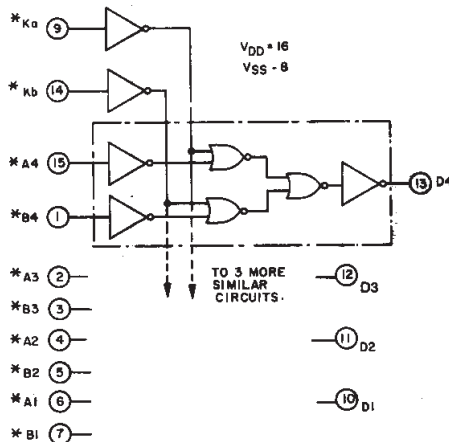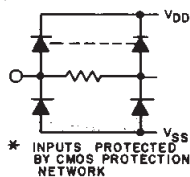| Ka	Kb	An	Bn	Dn
1	0	1	X	1
1	0	0	X	0
0	1	X	1	1
0	1	X	0	0
0	0	X	X	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

X = Don't Care

* INPUTS PROTECTED BY CMOS PROTECTION NETWORK

Fig. 1—Logic diagram.

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	Min.	Max.	Units
Supply-Voltage Range (For T_A = Full Package Temperature Range)	–	3	18	V

STATIC ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD} Max.	—	0,5	5	1	1	30	30	—	0.02	1	μA
	—	0,10	10	2	2	60	60	—	0.02	2	
	—	0,15	15	4	4	120	120	—	0.02	4	
	—	0,20	20	20	20	600	600	—	0.04	20	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	—	mA
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	—	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	—	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	—	
Output Voltage: Low-Level, V_{OL} Max.	—	0,5	5	0.05				—	0	0.05	V
	—	0,10	10	0.05				—		0.05	
	—	0,15	15	0.05				—	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	—	0,5	5	4.95				4.95	5	—	V
	—	0,10	10	9.95				9.95	10	—	
	—	0,15	15	14.95				14.95	15	—	
Input Low Voltage, V_{IL} Max.	0.5,4.5	—	5	1.5				—	—	1.5	V
	1,9	—	10	3				—	—	3	
	1.5,13.5	—	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	—	5	3.5				3.5	—	—	V
	1,9	—	10	7				7	—	—	
	1.5,13.5	—	15	11				11	—	—	
Input Current I_{IN} Max.	—	0,18	18	±0.1	±0.1	±1	±1	—	$\pm 10^{-5}$	±0.1	μA
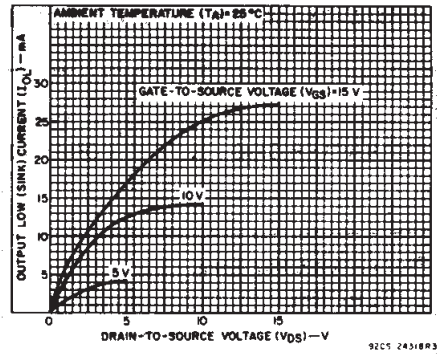
Fig. 2 — Typical output low (sink) current characteristics.
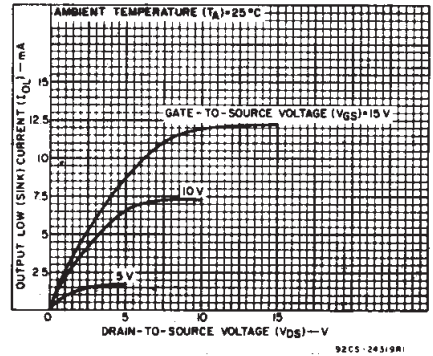

Fig. 3 — Minimum output low (sink) current characteristics.
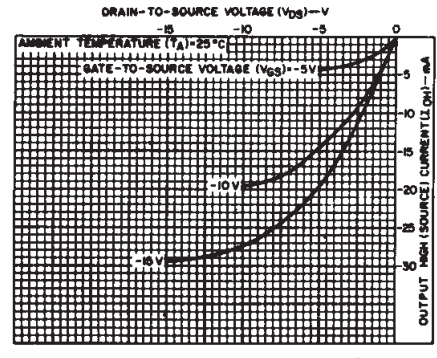

Fig. 4 — Typical output high (source) current characteristics.
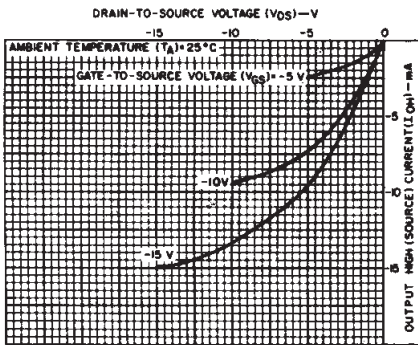

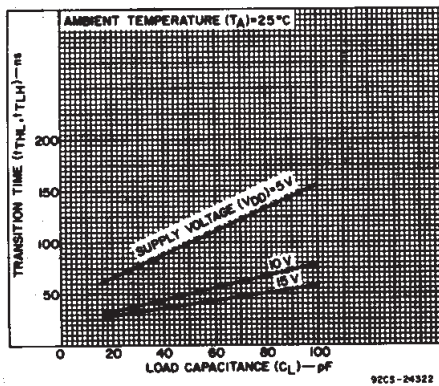Fig. 5 — Minimum output high (source) current characteristics.

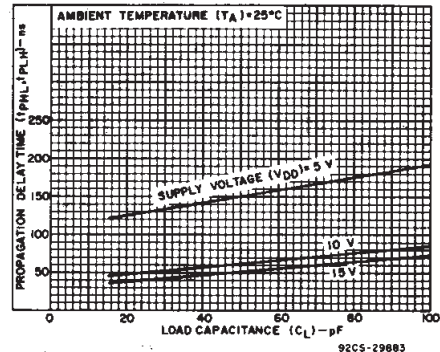Fig. 6 — Typical transition time as a function of load capacitance.

Fig. 7 — Propagation delay time as a function of load capacitance.

3

COMMERCIAL CMOS HIGH VOLTAGE ICs

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ C$, Input t_r, $t_f = 20$ ns, $C_L = 50$ pF, $R_L = 200$ kΩ

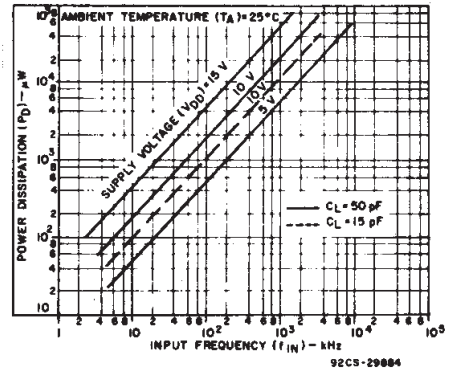| CHARACTERISTIC	TEST CONDITIONS		LIMITS			UNITS
		V_{DD} (V)	Min.	Typ.	Max.	
Propagation Delay Time; t_{PLH}, t_{PHL}		5	—	150	300	ns
		10	—	60	120	
		15	—	50	100	
Transition Time; t_{THL}, t_{TLH}		5	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
Input Capacitance, C_{IN}	All A and B Inputs		—	5	7.5	pF
	K_a and K_b Inputs		—	10	15	pF

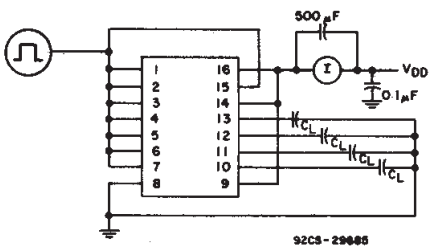Fig. 8 — Typical dynamic power dissipation as a function of input frequency.

Fig. 9 — Dynamic power dissipation test circuit.
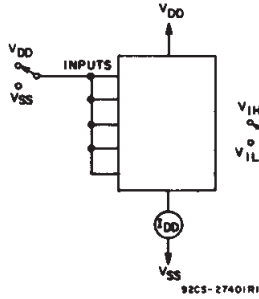
Fig. 10 — Quiescent device current test circuit.
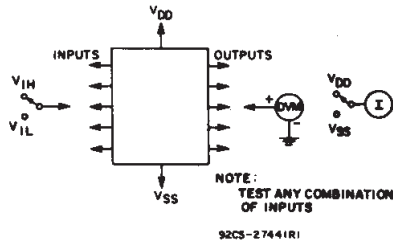
Fig. 11 — Input voltage test circuit.
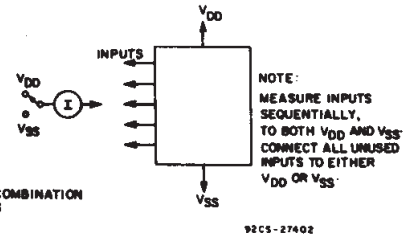
Fig. 12 — Input current test circuit.

TYPICAL APPLICATIONS
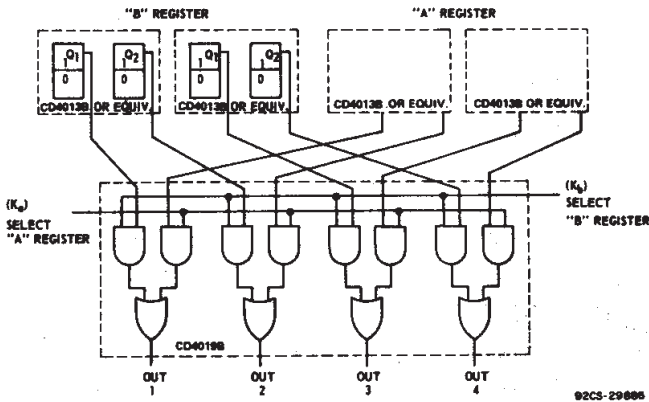
Fig. 13 — AND/OR select gating.
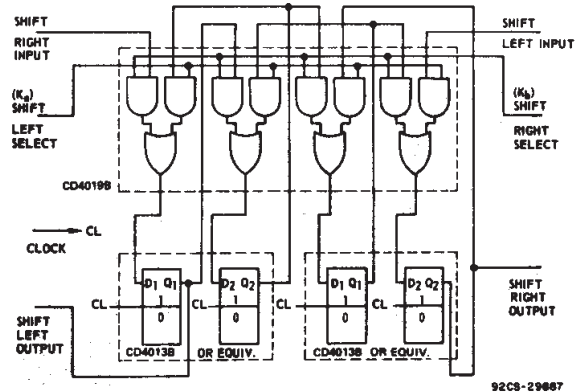
Fig. 14 — "Shift left/shift right" register.

CD4019B Types

TYPICAL APPLICATIONS (CONT'D)

TRUTH TABLE

K[·]	K [●]	OUT
0	0	0
1	0	A·B
0	1	A●B
1	1	A+B

92CS-29888
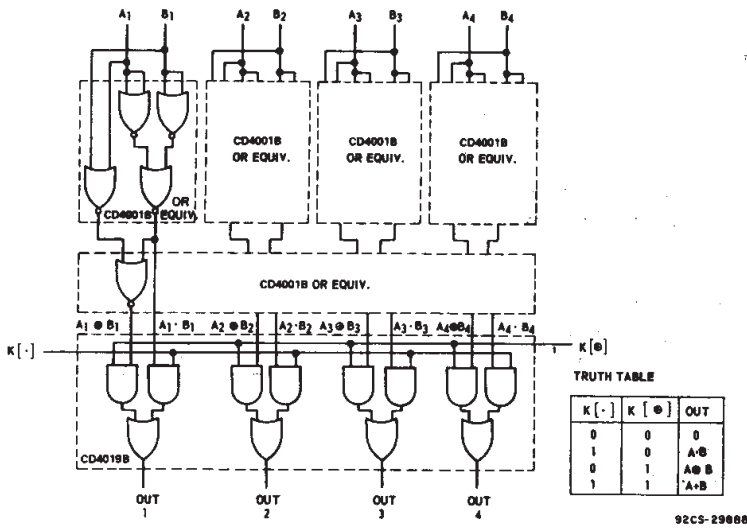
Fig. 15 — AND/OR Exclusive-OR selector.

92CS-29889

Fig. 16 — "True complement" selector.

3

COMMERCIAL CMOS
HIGH VOLTAGE ICs

92CS-36092

Dimensions and pad layout for CD4019BH

Dimensions in parentheses are in millimeters and
are derived from the basic inch dimensions as in-
dicated. Grid graduations are in mils $(10^{-3}$ inch).

PACKAGING INFORMATION

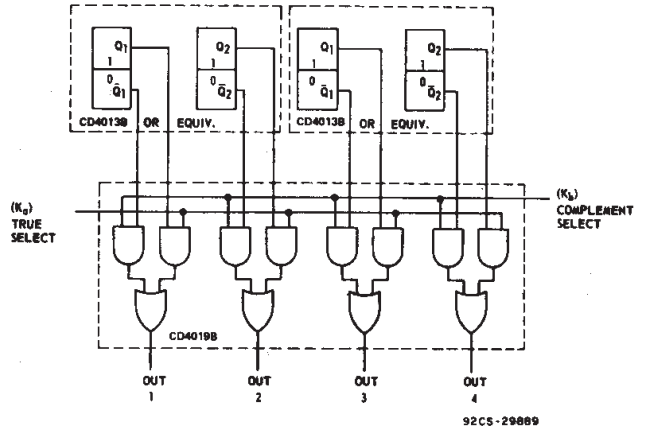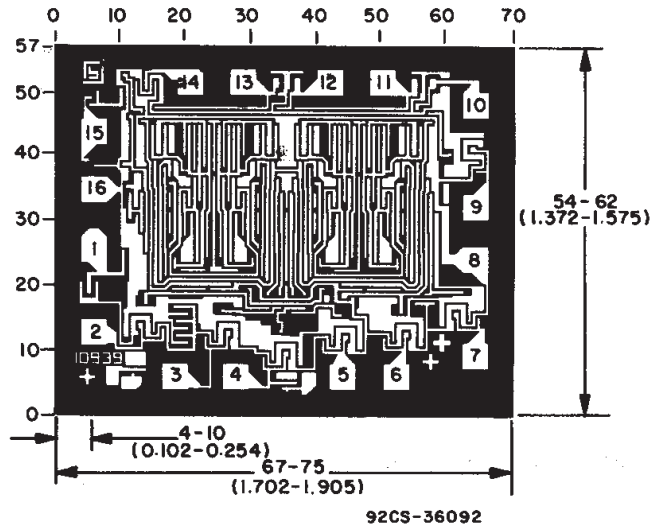| Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
CD4019BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD4019BEE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD4019BF	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
CD4019BF3A	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
CD4019BM	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4019BM96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4019BM96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4019BME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4019BMT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4019BMTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4019BNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4019BNSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4019BPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4019BPWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4019BPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4019BPWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
JM38510/05352BEA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DIM / PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

1   7

0.065 (1,65)
0.045 (1,14)

C

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

A

0°—15°

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

0.014 (0,36)
0.008 (0,20)

4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. This package is hermetically sealed with a ceramic lid using glass frit.
        D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
        E. Falls within MIL STD 1835 GDIP1—T14, GDIP1—T16, GDIP1—T18 and GDIP1—T20.

N (R−PDIP−T**)
16 PINS SHOWN

PLASTIC DUAL−IN−LINE PACKAGE

	PINS **	14	16	18	20
DIM					
A MAX		0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN		0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION		AA	BB	AC	AD

0.260 (6,60)
0.240 (6,10)

0.070 (1,78)
0.045 (1,14)

0.045 (1,14)
0.030 (0,76)

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)
Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
          B. This drawing is subject to change without notice.
          C. Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
          D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R−PDSO−G16) **PLASTIC SMALL−OUTLINE PACKAGE**

0.394 (10,00)
0.386 (9,80)

16

9

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)

1

8

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.007 (0,17)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)

0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−4/F 07/2004

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
        D. Falls within JEDEC MS−012 variation AC.

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

	PINS **	14	16	20	24
DIM					
A MAX		10,50	10,50	12,90	15,30
A MIN		9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A.   All linear dimensions are in millimeters.
           B.   This drawing is subject to change without notice.
           C.   Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G)**   **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN

DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

TEXAS
INSTRUMENTS
POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

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Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
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Mailing Address: Texas Instruments

Post Office Box 655303 Dallas, Texas 75265

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